

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended): A method of automatic power management control for Serial ATA interface, comprising:
  - (a) detecting an idle condition of said Serial ATA interface;
  - (b) measuring idle time of said Serial ATA interface with a power down counter when said Serial ATA interface is idle; and
  - (c) placing said Serial ATA interface into a first power saving mode when said idle time is equal to a first value,  
wherein an input clock counter counts an input clock and checks against a programmable value to generate a required frequency to operate said power down counter, said programmable value being held by a programmable register.
2. (original): The method of claim 1, wherein said first power saving mode is a Partial power state.
3. (original): The method of claim 1, wherein said first power saving mode is a Slumber power state.
4. (withdrawn): The method of claim 1, wherein said step (b) is performed by a power down counter whose frequency is determined by a programmable register based on input clock.
5. (original): The method of claim 1, wherein said step (c) comprising issuing a request for said first power saving mode to a physical layer of said Serial ATA interface by hardware when said idle time is equal to said first value.

6. (original): The method of claim 1, further comprising:
  - (d) placing said Serial ATA interface into a second power saving mode when said idle time is equal to a second value, wherein said first power saving mode is a Partial power state, and said second power saving mode is a Slumber power state.
7. (original): The method of claim 6, wherein said second value is greater than said first value.
8. (original): The method of claim 7, wherein said step (d) comprising issuing a request for Slumber power state to a physical layer of said Serial ATA interface by hardware when said idle time is equal to said second value.
9. (original): The method of claim 1, further comprising de-asserting a power down request when said Serial ATA interface is active.
10. (currently amended): An apparatus of automatic power management control for Serial ATA interface, comprising:
  - (a) means for detecting an idle condition of said Serial ATA interface;
  - (b) means for measuring idle time of said Serial ATA interface with a power down counter when said Serial ATA interface is idle; and
  - (c) means for placing said Serial ATA interface into a first power saving mode when said idle time is equal to a first value,  
wherein an input clock counter counts an input clock and checks against a programmable value to generate a required frequency to operate said power down counter, said programmable value being held by a programmable register.
11. (original): The apparatus of claim 10, wherein said first power saving mode is a Partial power state.
12. (original): The apparatus of claim 10, wherein said first power saving mode is a Slumber power state.

13. (withdrawn): The apparatus of claim 10, wherein said means (b) comprises a power down counter whose frequency is determined by a programmable register based on input clock.
14. (original): The apparatus of claim 10, wherein said means (c) comprises means for issuing a request for said first power saving mode to a physical layer of said Serial ATA interface by hardware when said idle time is equal to said first value.
15. (original): The apparatus of claim 10, further comprising:
  - (d) means for placing said Serial ATA interface into a second power saving mode when said idle time is equal to a second value, wherein said first power saving mode is a Partial power state, and said second power saving mode is a Slumber power state.
16. (original): The apparatus of claim 15, wherein said second value is greater than said first value.
17. (original): The apparatus of claim 16, wherein said means (d) comprises means for issuing a request for Slumber power state to a physical layer of said Serial ATA interface by hardware when said idle time is equal to said second value.
18. (original): The apparatus of claim 10, further comprising means for de-asserting a power down request when said Serial ATA interface is active.
19. (withdrawn): An apparatus, comprising:
  - a counter for counting idle time of Serial ATA interface;
  - a first programmable register holding a predetermined value, said first programmable register communicatively coupled to said counter; and
  - automatic power management circuitry communicatively coupled to said Serial ATA interface;

wherein said automatic power management circuitry issues a request for a power saving mode to a physical layer of said Serial ATA interface when a value of said counter is equal to said predetermined value.

20. (withdrawn): The apparatus of claim 19, wherein said power saving mode is a Partial power state.

21. (withdrawn): The apparatus of claim 19, wherein said power saving mode is a Slumber power state.

22. (withdrawn): The apparatus of claim 19, further comprising a second programmable register programmed based on input clock to determine frequency of said counter.

23. (withdrawn): The apparatus of claim 19, wherein said automatic power management circuitry comprising:

a first OR logic gate receiving BSY Bit, DRQ Bit and SERV Bit as input and outputting a first number indicating said Serial ATA interface being idle or active;

an inverter logic gate receiving said first number as input and outputting a second number to power down counter logic comprising said counter, wherein said Serial ATA interface being idle enables said power down counter logic to count down said idle time; and

power down/up circuitry communicatively coupled to said power down counter logic, wherein said power down/up circuitry issues a request for said power saving mode to said physical layer of said Serial ATA interface when a value of said counter is equal to said predetermined value.

24. (withdrawn): The apparatus of claim 23, wherein said automatic power management circuitry further comprising:

a second OR logic gate receiving said first number, Firmware Forcing WakeUp Bit, and a COMWAKE or COMRESET OOB signal as input, wherein said second OR logic gate outputs a WakeUp signal for disabling a

power down request to said power down/up circuitry when said first number indicates said Serial ATA interface is active, said Firmware Forcing WakeUp Bit is written in said automatic power management circuitry, and/or said COMWAKE or COMRESET OOB signal is detected;

wherein said power down/up circuitry de-asserts a power down request when said power down/up circuitry receives said WakeUp signal.

25. (withdrawn): An apparatus, comprising:
- a counter for counting idle time of Serial ATA interface;
  - a first programmable register holding a first value, said first programmable register communicatively coupled to said counter;
  - a second programmable register holding a second value, said second programmable register communicatively coupled to said counter; and
  - automatic power management circuitry communicatively coupled to said Serial ATA interface;
- wherein said automatic power management circuitry issues a request for Partial power state to a physical layer of said Serial ATA interface when a value of said counter is equal to said first value, and issues a request for Slumber power state to a physical layer of said Serial ATA interface when a value of said counter is equal to said second value.
26. (withdrawn): The apparatus of claim 25, wherein said second value is greater than said first value.
27. (withdrawn): The apparatus of claim 25, further comprising a third programmable register programmed based on input clock to determine frequency of said counter.
28. (withdrawn): The apparatus of claim 25, wherein said automatic power management circuitry comprising:
- a first OR logic gate receiving BSY Bit, DRQ Bit and SERV Bit as input and outputting a third value indicating said Serial ATA interface being idle or active;

an inverter logic gate receiving said third value as input and outputting a fourth value to power down counter logic comprising said counter, wherein said Serial ATA interface being idle enables said power down counter logic to count down said idle time; and

power down/up circuitry communicatively coupled to said power down counter logic, wherein said power down/up circuitry issues a request for Partial power state to said physical layer of said Serial ATA interface when a value of said counter is equal to said first value, and issues a request for Slumber power state to said physical layer of said Serial ATA interface when a value of said counter is equal to said second value.

29. (withdrawn): The apparatus of claim 28, wherein said power down/up circuitry issues a request for Partial power state to said physical layer of said Serial ATA interface when Firmware Forcing Partial Bit is written in said power down/up circuitry, and issues a request for Slumber power state to said physical layer of said Serial ATA interface when Firmware Forcing Slumber Bit is written in said power down/up circuitry

30. (withdrawn): The apparatus of claim 29, wherein said Firmware Forcing Partial Bit and said Firmware Forcing Slumber Bit are held by a fourth register.

31. (withdrawn): The apparatus of claim 28, wherein said automatic power management circuitry further comprising:

a second OR logic gate receiving said third value, Firmware Forcing WakeUp Bit, and a COMWAKE or COMRESET OOB signal as input, wherein said second OR logic gate outputs a WakeUp signal for disabling a power down request to said power down/up circuitry when said third value indicates said Serial ATA interface is active, said Firmware Forcing WakeUp Bit is written in said automatic power management circuitry, and/or said COMWAKE or COMRESET OOB signal is detected;

wherein said power down/up circuitry de-asserts a power down request when said power down/up circuitry receives said WakeUp signal.